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www.computingonline.net

Print ISSN 1727-6209
On-line ISSN 2312-5381
International Journal of Computing

# DIRECT DIGITAL FREQUENCY SYNTHESIZER IN THE RESIDUE NUMBER SYSTEM

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**Paper history:**
Received 20 March 2018
Received in revised form 11 August 2019
Accepted 10 September 2019
Available online 30 September 2019

**Keywords:**
RNS;
Adder;
DDS;
CORDIC;
CRT.

**Abstract:** The principles of construction and operation of direct digital frequency synthesizers are considered in order to speed up computational operations using Residue Number System. The problems of forming the output signals are considered. The specifics of the implementation of the operation of direct and reverse transformations from positional to non-positional number systems are described. A mathematical model of a synthesizer with a phase accumulator in a Residue Number System is considered. Methods for converting from RNS (Residue Number System) to binary system for problematic operations are considered. The design of a DDS (Direct Digital Synthesizer) with a phase accumulator in a Residue Number System and a converter to an analogue signal form is proposed without the use of slow ROM (Read Only Memory). The article deals with the issues of efficiency of the crystal area of the synthesizer and the reduction of the delays in the formation of the output signal.



## 1. INTRODUCTION

An important problem of direct digital synthesis arising in digital systems of frequency synthesis and signals is the speed of processing the values of samples of synthesized signals, the speed of data processing and, in turn, the energy efficiency of such systems. The problem of distortion in the output spectrum of a direct digital frequency synthesizer has been considered in detail in [1]. The basic idea of the DDS is to preserve the values of the harmonic function in a permanent storage device and consistently read these values with different phase steps to obtain the required frequency of the output harmonic signal. In some cases, a permanent storage device replaces a combined device containing an additional interpolator, which allows you to reduce the amount of ROM (Read Only Memory), but leads to increased distortion of the spectrum of the output signal of the digital frequency synthesizer [2].

However, in any case, to ensure the accuracy of the synthesis of the output frequency, it is necessary to increase the bit rate and the speed of the synthesizer core, which is built on the basis of a cumulative adder. For this purpose, cumulative adders of complex architecture are used, as shown in the work [3]. However, the use of traditional number systems with sequential transfer between bit positions with increasing synthesized frequency encounters with increasing time of signal propagation and reduction of the maximum possible synthesized frequency. Therefore, it was proposed to use non-positional number systems to increase the maximum synthesized frequency with the storage of the digits of the cumulative adder [4].

Accuracy and speed, required for a large number of calculations in the process of digital applications, have a significant effect on the quality of synthesized signals. The main ways to solve these problems is the modernization of digital synthesis systems by using more efficient methods of calculation [5].

Taking into account the requirements for building high-performance computing devices, including those applicable in digital frequency and signal synthesis systems, the main method for solving the problem of increasing the speed of digital data being processed is confirmed, namely, a method that allows building the structure of a computing device of such a system with the maximum parallelization of performing arithmetic operations. This method, in turn, solves a number of tasks that must be performed by the computing device:

- Introduction of efficient algorithmic and hardware structures of parallel type.
- Ensuring a high degree of integration and unification of the arithmetic unit.
- Application of advanced error control.
- Use of variants of computer arithmetic, which are best suited for high-speed implementations of computational processes that require large amounts of computation [6].

The use of the usual binary number system in the course of performing arithmetic operations over a large amount of data entails a number of difficulties caused by the presence of inter-bit relationships. This disadvantage imposes limitations on the ways of implementing arithmetic operations, thereby complicating the hardware and limiting the system's performance [7]. Therefore, it is expedient to use such arithmetic, in which the bitwise relations in the calculations were absent or were minimized. The arithmetic possessing the specified properties is the non-positional number system Residue Number System (RNS). Thus, the search for ways to solve the problem of increasing productivity led to the idea of independent parallel processing of data and, consequently, to the replacement of the usual binary system with the system of residual classes [8].

In this system, the numbers are represented by their remainders from dividing by the chosen base system, and all rational operations can be performed in parallel to each of the digits. However, Residue Number System that is so convenient on the one hand, has a number of shortcomings on the other hand: the limited effect of this system on the field of positive integers, the difficulty in determining the ratio of numbers in residual expression, determining the outcome of an operation from a range, etc. Thus, effective ways should be found to eliminate these shortcomings [9].

## 2. RESEARCH METHOD

In the RNS the numbers are represented by mutually prime numbers which are called modules $\beta = \{p_1,...p_k\},\ GCD(p_i, p_j) = 1$ where $i \neq j$. The product $P = \sum_{i=1}^{k} p_i$ of all modules RNS is called – dynamic range of the system. Any integer number in the range $0 \le X \le P$ can be uniquely represented in the RNS as the vector $\{x_1, x_2,...., x_k\}$, where $x_i = |X|_{p_i} = X \bmod p_i$ [2].

Dynamic range of RNS is usually divided into two approximately equal parts, so that approximately half of the dynamic range is represented by positive numbers, and the rest of the dynamic range – negative. So, each integer satisfying one of the following two relations:

$$\begin{aligned} -\frac{P-1}{2} \le X \le \frac{P-1}{2}, \text{ for odd } P, \\ -\frac{P}{2} \le X \le \frac{P}{2}, \text{ for even } P, \end{aligned} \quad (1)$$

may be presented in the RNS.

The operations of subtraction, addition and multiplication in RNS are represented by formulas:

$$\begin{aligned} A \pm B = (\alpha_1, \alpha_2,...\alpha_n) \pm (\beta_1, \beta_2,...\beta_n) = \\ ((\alpha_1 \pm \beta_1) \bmod p_1, (\alpha_2 \pm \beta_2) \bmod p_2,. \\ .., (\alpha_n \pm \beta_n) \bmod p_n) \end{aligned} \quad (2)$$

$$\begin{aligned} A \times B = (\alpha_1, \alpha_2,...\alpha_n) \times (\beta_1, \beta_2,...\beta_n) = \\ ((\alpha_1 \times \beta_1) \bmod p_1, (\alpha_2 \times \beta_2) \bmod p_2, \\ ..., (\alpha_n \times \beta_n) \bmod p_n). \end{aligned} \quad (3)$$

Equations (2) – (3) show the parallel nature of the RNS, free from bit transfers. These operations are called modular, since for their processing it is necessary to operate with small numbers (residues) arising as a result of division into a set of modules, and for obtaining numerical values only one clock cycle is required [10]. To convert numbers from the binary positional number system to RNS we use an algorithm based on the application of a distributed arithmetic. *K*-bit number *X* is divided into separate formats, for each of which is assigned a pre-known number of *B*-binary discharges. Then the *n*-bit binary number can be expressed as a combination $\frac{n}{B}$ - positional formats with the dimension *B* bits.

This position of each format is assigned a specific weight $2^j$, where $j = 0, B, 2B, ..., MB$

$$X = \sum_{j=0}^{M} (\sum_{i=0}^{B-1} x_i 2^i) 2^j ,$$

where $B$ – a number of digits of the selected format; $M$ – the degree of the format; $x_i$ - a factor of 0 or 1; $j = 0, B, 2B, ..., MB$ - the position of the format; $i$ - the position of the digit in the format. Conversion of a number from binary positional code into the modular code is carried out using a modular addition of the remainders modulo $m_i$:

$$X = \left| \sum_{j=0}^{M} (\left| \sum_{i=0}^{B-1} x_i 2^i \right|_{m_i}) 2^j \right|_{m_i} .$$

Restoring the number $X$ by the remainders $\{x_1, x_2, ...., x_k\}$ is based on the Chinese remainder theorem

$$X = \left| \sum_{i=0}^{k} \left| P_i^{-1} \right|_{p_i} P_i \right|_p , \quad (4)$$

where $P_i = \frac{P}{p_i}$. Element $\left| P_i^{-1} \right|_{p_i}$ means a multiplicative inverse for $P_i$, by module $p_i$ [2].

The advantages of representing numbers in RNS can be represented as follows:

1. Since there is no propagation of transfer between arithmetic blocks in the RNS, and numbers of large dimension are represented as small residues, this leads to increase in speed of data the processing.
2. When presenting data using RNS, a large number of numbers are encoded in a set of small numbers of residues, and, accordingly, the complexity of computing devices in each channel modules is reduced, which facilitates and simplifies the operation of the computer system.
3. The RNS is a non-positional system without the lack of dependence between its arithmetic blocks; therefore, an error in one channel does not extend to others, which in turn, facilitates the process of detecting and correcting errors.

Thus, the use of RNS makes it possible to simplify and reduce the architecture of electronic computing devices, thereby increasing not only the speed, but also the energy efficiency of products.

However, operations such as comparison of two numbers, division and detection of a sign are laborious and expensive in RNS. Many solutions have been proposed to these problematic operations. Most of them include converting the remainder into a binary system (the inverse transformation). On the other hand, choosing a proper set of modules is another important issue for building an effective RNS with a sufficient dynamic range.

## 3. RESULTS AND ANALYSIS

Summing up some results, it can be noted that Residue Number System allows for significantly improving the parameters of a computer in a Direct Digital Synthesizers (DDS) in comparison with a computer built on the same physical and technological basis, but in a positional number system, and also to receive new more progressive constructive and structural solutions.

The essence of a digital frequency synthesis is the conversion of the digital code of the number $A$ into an analogue harmonic signal with a frequency

$$f_{out} = \frac{F_{CLK} \cdot A}{M}, \ 0 \le A \le M , \quad (5)$$

where $F_{CLK}$ – frequency of the clock generator; $M$ is a fixed positive integer, based on the application of the periodicity property of a harmonic function analogous to the property of arithmetic operations modulo the ring of integers.

In the proposed device, the formation of a harmonic oscillation $X(t) = U \cos(2\pi f_{out} t)$ is carried out by obtaining its samples at times $t = \Delta t \cdot k$ with the clock frequency $F_{CLK} = 1/\Delta t$.

Taking into account (5), the discrete samples of a harmonic oscillation with amplitude $U$ are described by the expression:

$$\begin{aligned} &X(\Delta t \cdot k) = U \cdot \cos(2\pi f_{out} \cdot \Delta t \cdot k) = \\ &U \cdot \cos\left( 2\pi F_T \cdot \frac{A}{M} \cdot \Delta t \cdot k \right) = \\ &U \cdot \cos\left( \frac{2\pi A k}{M} \right), \end{aligned} \quad (6)$$

where $k = \overline{0, \infty}$. Since the cosine is a periodic function, then

$$\left( \frac{2\pi k}{M} \right) \bmod 2\pi = \frac{2\pi}{M} (k) \bmod M .$$

Therefore, $k$ can be formed within the period $k = \overline{0, M-1}$. An arbitrary nonnegative integer $A$ can be represented in the code of the Residue Number System. The integer $A$ in the range

$0 \le A \le \prod_{i=1}^{N} m_i$ is uniquely coded by its residues $a_i$ on the bases $m_i$:

$$A = (a_i, a_2, ..., a_N),$$

where

$$a_i = A - \left[\frac{A}{m_i}\right] \cdot m_i = (A) \bmod m_i;\ [\bullet] -$$

the integer part of a number; $m_i, m_2, ..., m_N$ – a set of relatively prime positive integers, called bases; $N$ – a number of bases.

The code in the RNS of the result of the product $C$ of the numbers $A$ and $k$ is determined by computing the individual products of the residues for each base:

$$A \cdot k = C[k] = (c_1[k], ..., c_N[k]) = ((a_1 \cdot \chi_1) \bmod m_1, ..., (a_N \chi_N) \bmod m_N),$$

where $c_i[k] = ((a_i \cdot \chi_i) \bmod m_i, \quad i = \overline{1, N}/$ We represent (6) in the form

$$X(\Delta t \cdot k) = U \cdot \cos\left(\frac{2\pi}{M} \cdot C[k]\right) = U \cdot \cos\left(\frac{2\pi}{M} \cdot (C[k]) \bmod M\right). \quad (7)$$

A discrete samples, directly proportional to the (7) can be formed in the agile modular adder [11].

Fig.1 shows a block diagram of a high-speed direct digital frequency synthesizer with a flexible architecture.

The Phase Accumulator (shown below in Fig.1.) performs modulo $M$ addition where $m_1 = 2^{P+2}$ for non-negative $p$. It consists of $n$ finite state machines (FSM) performing phase accumulation modulo $m_i$. In [11] recommends the use of a finite state machine in place of modulo adder for the phase accumulator, since the delay can be of only two logic levels. The input to finite state machine is the binary encoded *i*-th residue digit $|k|_{m_i}$ of the frequency setting word. The state of finite state machines in the time is the binary encoded *i*-th residue digit of the phase at that time.

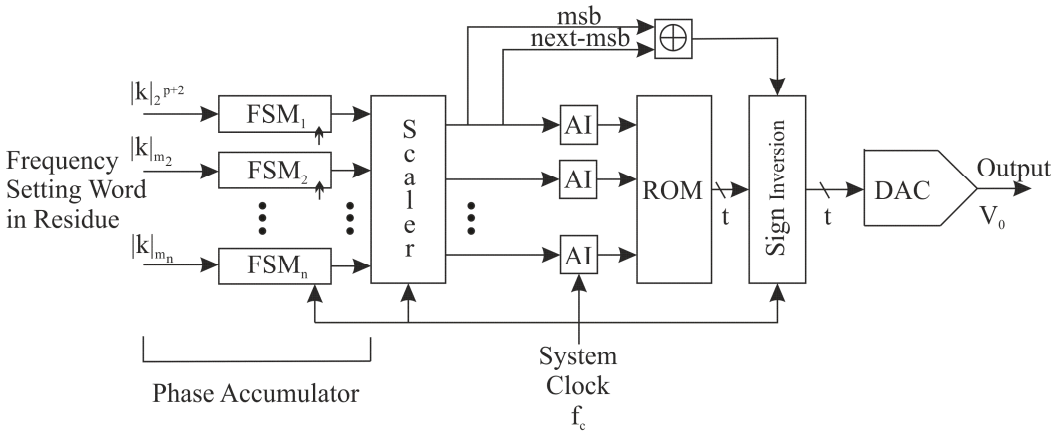


**Figure 1 – Frequency Agile Direct Synthesizer [11]**

The values of the phase words entering the DAC (Digital to Analogue Converter) can be calculated on the basis of the CRT (Chinese Remainder Theorem) on the residues. The inverting unit of the phase-word address (AI) in Fig. 1 performs an additional inverting by modulus $m_i$ so that it can achieve the symmetry of the output harmonic signal.

But the author of work [9] has convincingly proved that in such a structural scheme the use of a permanent storage device with values of the sine function is impossible.

The correct solution is to save the results of the transformation of the harmonic CRT function into the ROM, where the value of the residues remains. Accordingly, inverting blocks (AI), the value of the higher bit in the architecture of the high-speed direct digital frequency synthesizer in Fig. 1 are also not useful because of the lack of symmetry information. It is clear that in the proposed structural scheme of the synthesizer the size of the permanent storage device will increase significantly. Thus, the increase in speed, as can be seen from the analysis of the synthesizer, occurs in the phase accumulator, which has a smaller length of the phase word than binary systems, and the scaling of the harmonic function actually introduces additional operations, reducing

the speed of the synthesis of signals, respectively, makes it possible to reduce the required volume of ROM. However, note that a ROM that corresponds to a certain balance uses as the address all bits of a word. Inversion blocks and exclusive blocks OR for older and subsequent bits are also not required [12].

In addition to the classical DDS structure, there is number of methods for converting the values of the phase accumulator into a harmonic waveform. We analyzed the existing methods; the results of this analysis of the most common methods are given in Table 1.

These methods can be implemented in the RNS, separately one can single out the method of Taylor series approximation [13,14] and the CORDIC (COordinate Rotation DIgital Computer) algorithm [15-18]. In these methods, multipliers are used the whose implementation in the RNS system is much more efficient than in the binary system. In [19] an even simpler method for synthesizing a harmonic signal of a given frequency from the values of the phase accumulator was proposed. The most effective approach in terms of reducing the crystal area of a synthesizer of direct digital synthesis is the use of blocks of amplitude-phase conversion without the use of a ROM.

**Table 1. Comparative table of different methods of phase-amplitude transformation with a resampling level of -85dB**

| Method | Memory capacity | Coefficient of compression | Additional required chips | Retraction achieved in model | Note |
|---|---|---|---|---|---|
| Classic method | $2^{14} \times 12$ bit | 1:1 | - | -97,23 dB | - |
| Sunderland Architecture | $2^8 \times 9$ bit<br>$2^8 \times 4$ bit | 59:1 | Adder | -86,91 dB | Simple implementation |
| Nikola's architecture | $2^8 \times 9$ bit<br>$2^8 \times 4$ bit | 59:1 | Adder | -86,81 dB | Simple implementation |
| Approximation in Taylor series with two additions | $2^7 \times 9$ bit<br>$2^7 \times 5$ bit | 110:1 | Adder multiplier | -85,88 dB | The need for a multiplier |
| Algorithm CORDIC | - | - | 14 states, 18 bit – length of internal transformation | -84,25 dB | Great computational complexity |

In Fig. 2 the functional diagram of the proposed direct digital frequency synthesizer without ROM is presented. DDS replaces the ROM and the linear DAC on a sine-weighted digital-to-analogue converter that serves as a phase-amplitude conversion unit and at the same time, it is a DAC. This solution leads to the fact that there is no need for ROM with a relatively low speed and which is a bottleneck for DDS high-speed. An important issue to be solved in such a synthesizer scheme is the construction of a sinus-weighted DAC with a nonlinear distribution of segments in the phase-amplitude converter.

We considered the ways of designing a digital phase-frequency synthesizer with a phase accumulator in the system of RNS and sinus-weighted type of DAC. Such a combination of functional units has not previously been used in the design of direct synthesis synthesizers and, according to our opinion, represents the scientific novelty. In traditional schemes, the conversion of the remainder to analogue occurs in several stages, where the conversion to a binary system is one of the stages. This procedure worsens the speed of the whole RNS system by adding additional constraints and increasing the waiting time for the conversion result. Therefore, a direct remainder to analogue converter is sought to solve that problem and make the RNS efficient. The problem of direct transition from the rest to the analogue is not yet sufficiently worked out in modern works. In [19], the author proposed his way of solving the problem, namely, a direct analogue converter, based on a mixed radix system.

The main disadvantage of the converter on the basis of the mixed radix system is the sequential algorithm of work, which is slow for a large dynamic range of frequencies. We propose to use a combination of a phase accumulator built in Residue Number System to a digital-to-analogue converter with a direct transformation into a harmonic signal based on the CRT. Such a converter eliminates the need for an intermediate stage of conversion into a binary system of calculation and can be much more productive than the direct converted residue-to-binary system. Consequently, there is no more need for a large area modular adder. Instead, the summing operational amplifier is used to perform a modular addition in the analogue form. The proposed converter facilitates the realization of CRT in the

need for direct conversion into analogue form and is suitable for systems with a wide dynamic range.

CRT is not a sequential algorithm, as opposed to the mixed radix system. The value of each balance can be generated simultaneously using the ROM search tables. Consequently, the proposed architecture for direct conversion from RNS to an analogue form is presented in Fig.3.

The synthesizer consists of the following functional units: the binary code converter into the RNS, the phase accumulator in the RNS, the RNS processor, the conversion units based on the CRT, the DAC units and the summing operational amplifier. The frequency control word (FCW) is fed to the binary code converter in the Residue Number System. In the phase accumulator, the phase values are accumulated for each of the residues in the RNS. In the RNS processor, the necessary transformations of signals such as phase transformation, amplitudes, modulation of the synthesized oscillation occur. After this, the received signal in the form of its values in the RNS enters separately into conversion units based on the CRT system. The resulting values are converted into an analogue form in the DAC units [19].

To find the necessary balance partial sums are added to the analogue converter in the phase accumulator, the algorithm works on the basis of permanent storage devices of small size. The volume of the ROM for partial sums will be $(2^k \times 3k)$ -bit ROM in the case where the size of the residue is a $k$ bit.

The value of each partial amount is converted into an analogue form by a separate digital-to-analogue converter. Then, the final addition of analogue values of partial sums in a single analogue adder based on the add-amplifier is carried out.

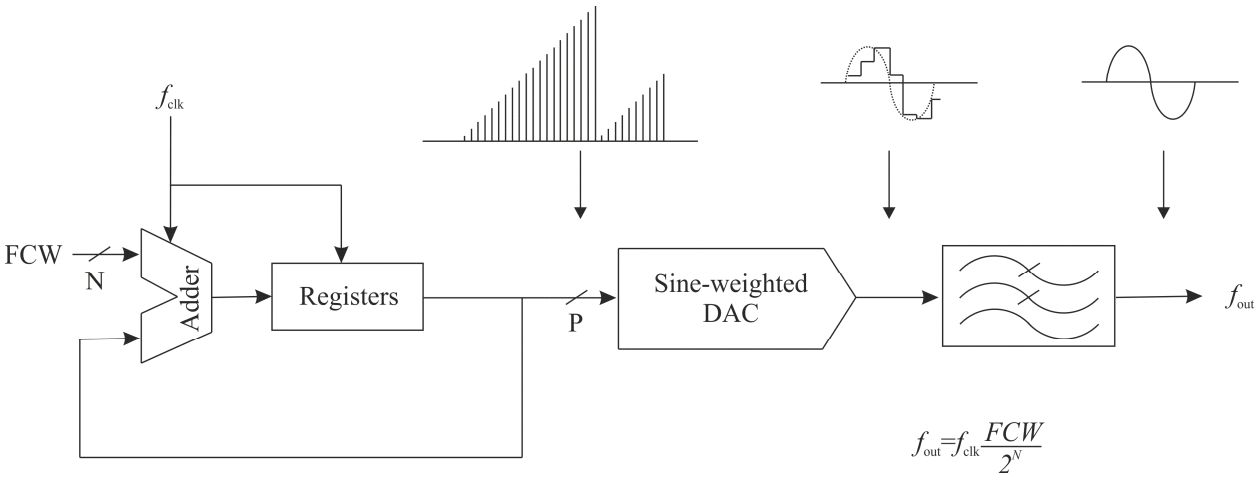


**Figure 2 – Structural scheme of the ROM-free DDS [19].**

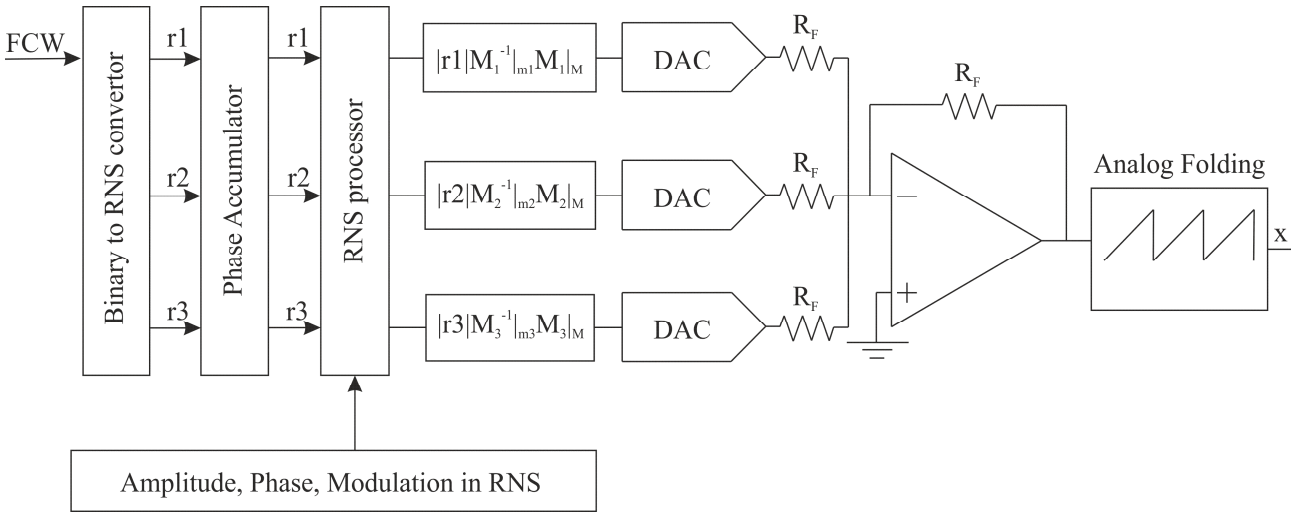


**Figure 3 – Structural scheme of the RNS ROM-free DDS**

The delay in the complete conversion of the synthesized signal is

$$t_{all} = t_{rom} + t_{DAC} + t_{adder} . \quad (8)$$

For large residual values – $k$, the size of the ROM begins to increase and at a certain stage becomes a bottleneck for increasing the speed of DDS. The ROM area is of critical importance for the construction of high-speed DDS. The proposed DDS will consume power comparable to the converter described in [20].

RNS DDS with a traditional R/B (Residual-to-Binary) converter and DAC will be less effective than the proposed structure due to the significant loss of speed of the residue to binary number system converter. The speed of work proposed by us RNS ROM-free DDS will be roughly higher in proportion to the number of partial DACs (see Fig. 3). However, the increase in the number of DACs leads to increased distortions of the synthesized signal.

In the RNS ROM-free DDS synthesizer, the output form of the DDS signal will be distorted from phase and amplitude distortion due to a small number of quantization levels in the DACs. Also, there will be side effects of components in the spectrum of the output signal that are inherent to all DDS synthesizers. The form of distribution of the components of the output spectrum of the DDS signal can be found by the corresponding analytical expression

$$f_E = f_{clk} \cdot \frac{2^{N-1} \bmod (2^{N-1} - 1)}{2^{N-1}} = f_{clk} \cdot \left(\frac{1}{2}\right)^{N-1},$$

where $N$ is the bit length of the main frequency word before transformation into Residue Number System. We analyzed the phase noise models of the proposed synthesizer. From the analysis it can be concluded that the spectral density of phase noise power RNS DDS can be represented as a sum of three components: the spectral density of phase noise of the clock generator, quantization noise and the noise of the synthesizer elements:

$$S_{outDDS}(F) = S_T(F) K_{DDS}^2 + S_{qn}(F) + S_{own}(F),$$

where $K_{DDS}^2 = (f_{out} / f_T)^2$ - the coefficient of transmission of DDS by noise, $f_T$ and $f_{out}$ - the clock and output frequencies, – the frequency offset from the carrier. The phase noise analysis of RNS DDS has shown that they have additional deviations (up to 5dB/Hz) compared with the experimental noise characteristics of modern integral DDS.

## 4. CONCLUSION

A direct digital synthesizer (DDS) with phase accumulator and residue-to-analogue converter based on the Chinese remainder theorem was proposed. It was proposed a new structural scheme of RNS DDS without transforming into a binary representation form. The proposed RNS DAC implements the Chinese theorem on the residues with the help of analogue circuit elements and is most suitable for the implementation of the DDS.

The proposed residue-to-analogue converter was compared to the residue-to-analogue converter, based on the mixed-radix conversion and to the residue-to-binary converter based on the CRT. The key features of the proposed residue-to-analogue converter are:

- The proposed solution made it possible not to use large modular adders, which occupy a large area on the crystal. Instead, it uses rather simple manufacturing and designing amplifiers.
- The proposed architecture reduces the size of the ROM that is a very important factor in designing direct digital synthesizers for fast switching.

The structure of a perspective synthesizer of direct digital synthesis is analyzed. The values of the potential Spurious-Free Dynamic Range and methods for its improvement are analyzed.

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