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SYNTHESIS AND FPGA–IMPLEMENTATION BASED NEURAL TECHNIQUE OF A NONLINEAR ADC MODEL

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Abstract: *The aim of this paper is to introduce a new architecture using Artificial Neural Networks (ANN) in designing a 6-bit nonlinear Analog to Digital Converter (ADC). A study was conducted to synthesise an optimal ANN in view to FPGA (Field Programmable Gate Array) implementation using Very High-speed Integrated Circuit Hardware Description Language (VHDL). Simulation and tests results are carried out to show the efficiency of the designed ANN.*

Key-words: *Linearization, ADC, Artificial neural network, VHDL, FPGA-implementation.*

1. INTRODUCTION

The main requirement in measurement is to generate an electrical signal proportional to the input physical quantity with certain accuracy. However, a practical sensor does not realize the ideal signal transfer, but exhibits nonidealities like offset, gain and nonlinearity, in addition to the possible effects of disturbing variables which affect the desired sensor response to the physical quantity of interest. Linearity is often the characteristic that limit performances of some low cost sensors which present high repeatability and good stability.

Emerging techniques such as neural network technique have been widely investigated in order to respond to fast and easy data acquisition systems. The architectures proposed in [1], [2] and [3] deal with the use of neural networks in order to linearize the nonlinear characteristics of sensors. These approaches give good results contrary to the classical electronic methods [4], for which they are complex and limited to reduce the influence of perturbations. Also, Flash A/D converters have been designed with neural architectures where the circuitry complexity was reduced [5], [6] and [7].

Motivated by reducing the complexity and the cost of the measurement system, a simplified neural architecture is chosen to synthesize both of the two functions of the measurement chain: linearization and analog to digital conversion. In other words, neural network with one hidden layer have been chosen and trained to learn the combined architecture. The architecture proposed in this paper requires only 63 neurons in the hidden layers and the design of this latter is realized with the aim of FPGA implementation.

FPGAs are becoming increasingly popular for prototyping and designing complex hardware systems [8]. The structure of a FPGA can be described as an array of blocks connected together via programmable interconnections. The choice to build a neural network in digital hardware comes from several advantages such as an easy weights storage, a low sensitivity to electric noise and temperature and well understanding the design principles that have lead to new powerful tools for digital design with *VHDL* [9].

However, the main goal of this work is the minimization of the neurons number and the optimization of the synthesized neural circuit, in view to FPGA-implementation. It is shown from our experience that the weights obtained in the training phase for the LSB are partly used to synthesize all the other bits [6], where some hidden neurons of the LSB *ANN* contribute in the entire nonlinear neural ADC. Simulation and tests results are given to test the efficiency of the partially implemented nonlinear ADC.

2. THE PROPOSED APPROACH

The chosen sensor in this application is a commercial thermistor (NTC) and Fig.1 shows the characteristic which has been raised experimentally with a simple calibration procedure.

Initially, to synthesize a 6-bits nonlinear neural ADC converter, six neural networks have been chosen, the initial global architecture is composed by a single input and six outputs where each output has its own neural network with one hidden layer, Fig.2 shows the initial proposed architecture [10]. Each neural network is trained independently and depends on the significance of the bits. V_{in} represent the analog signal to be converted issued from the NTC bridge.

To simplify and optimize the FPGA implementation, the activation function σ chosen for each neurons in the whole architecture is the hyperbolic tangent with high slope equal to 30 ($\sigma(x)=\tanh(30x)$), in practice, this activation function is the heaviside function (comparator).

Like any ANN modelization, three phases are followed: learning phase, validation phase and testing phase [11]. The learning phase is realized with the backpropagation algorithm using Neural Network Toolbox of Matlab and follows a strategy to identify the neural network for every bit.

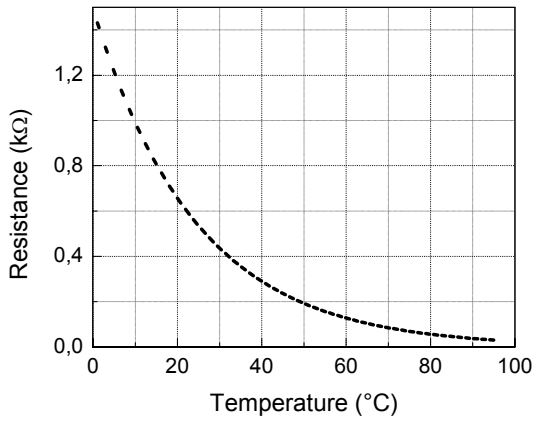

Fig. 1–Thermistor characteristic.

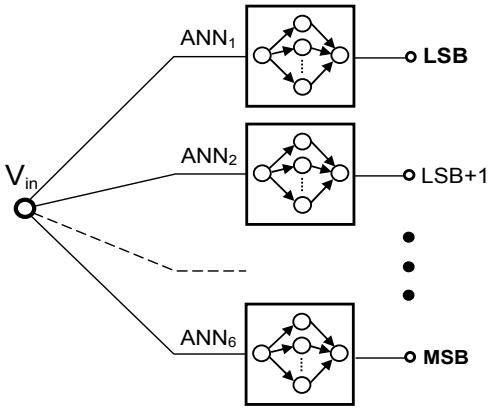

Fig. 2–The initial proposed neural architecture.

The results of the learning phase are shown in Table.1 where 120 neurons are needed in the hidden layers.

After observing and analyzing the weights file, an appropriate architecture for the whole ANN was concluded. The function required to generate a ANN_i (i= 2 to 6) can be deduced from the function which is necessary to generate the ANN_1. In the proposed nonlinear neural ADC the new architecture are such that the hidden layer of the higher significant bits are included in the lower significant bit (LSB only), thus

$$ANN_{H6} \subset ANN_{H5} \subset \cdots \subset ANN_{H1}$$

where ANN_{Hi} is the hidden layer of the ANN_i and ANN_1 corresponds to the LSB. However, this proposed architecture provides simplicity and optimization and as shown in Fig.3, ANN_i can be partly found in ANN_1. With this optimized architecture, the number of neurons in the hidden layer is reduced to 63 from 120 obtained with the initial architecture.

Table 1. Results of the learning phase

Bit	MSB	LSB+5	LSB+3	LSB+2	LSB+1	LSB
ANN	ANN_6	ANN_5	ANN_4	ANN_3	ANN_2	ANN_1
Neurons	1	3	7	15	31	63
Iterations	0	10^4	3.5×10^5	5×10^6	2.5×10^7	3×10^8
MSE	–	7×10^{-6}	3×10^{-5}	7×10^{-5}	9×10^{-5}	1×10^{-4}

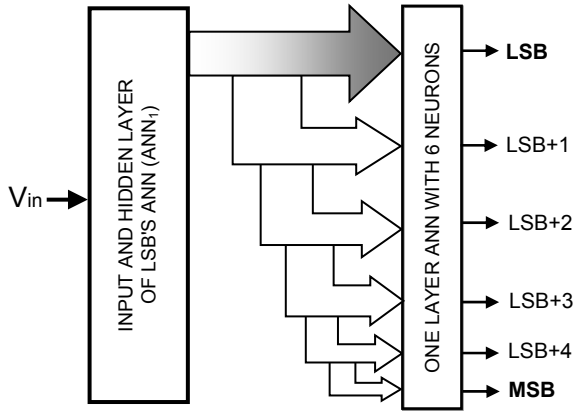

Fig. 3–Optimized ANN architecture.

3. ANN CIRCUIT ELEMENTS

Some hardware constraints must be taken into account. In order to develop realistic devices with a convenient accuracy and a reasonable hardware size, the resolution of the weights and calculus must be redefined. So the optimization of the architecture and the reduction of the number of configurable

logic blocks (CLB) used in the FPGA circuit implicate the best accuracy obtained during the learning phase.

The design approach was modular to accommodate higher order problems with increased resolution in the digital implementation. The overall design was created and simulated in *VHDL* program using ISE 6.2i *Xilinx* software. The basic unit of the synthesized *ANN* is the neuronal model of *Mc Culloch and Pitts* [12] where the mathematical model is represented by Eq.1,

$$y = \sigma\left(\sum_{i=1}^{N} w_i x_i + b_l\right) \quad (1)$$

Where N–number of the neuron's inputs, b_i –biais input, w_i –synaptic weights, σ –activation function.

Hence, the fundamental functions are the multiplication of the inputs by synaptic weights, the summation and the activation function. In the *VHDL* corresponding program, the sum is realized with a serial adder, the two's complement serial-parallel multiplier is used for the multiplication and the activation function is simply a comparator. The inputs and weights are represented using a special 8 bits encoding technique [13] where 1000000 represents 4 and 00000001 represents 0.03125 various numbers are represented by simply adding these values together (Table.2). A ninth bit is used as a sign bit (0 for minus and 1 for plus). Therefore the smallest number which can be represented is -7.96875 (0 1111 1111) while the largest number is 7.96875 (1 1111 1111).

Table 2. Representing values

Value	Encoded value	Data representation
0.2564	0.25	1 0000 1000
-3.5264	-3.53125	0 0111 0001
5.7861	5.78125	1 1011 1001

A serial adder consists of a full adder and flip-flops on the adder's output and carry. Using one cell of an iterative implementation of an adder, the serial adder can add any arbitrary value of length n in n clock cycles (Fig. 4).

The serial parallel multiplier implements an add-shift arithmetic with a resource sharing methodology. Each bit of the multiplier utilizes the same logic cells. The multiplicand is presented to the circuit in parallel with the least significant bit (LSB) first. The result is bit-serial, also with the LSB first, allowing the multiplier to be cascaded with more serial parallel multipliers (Fig.5). The number of the parallel inputs determines the size required by the multiplier circuit.

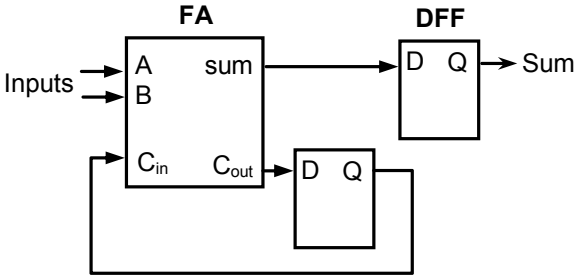

Fig. 4–Bit serial adder (FA represents the full adder and DFF denotes the D flip flop).

4. FPGA IMPLEMENTATION

Actually, the synthesis tools allow the use of FPGA resources with schematics entrance as well as an algorithmic one. The algorithmic design is written with *VHDL*. This language permits the design of complex circuits with structural description or a behavioral one.

Fig. 6 shows all the information relative to design flow and tools. The synthesis software leads from a VHDL program and after compilation to an *XNF* (Xilinx Netlist Format) file used by *Xilinx* tool, and the corresponding schematics by means of primitive and X-blocs components with a logic optimization. The functional simulation insures of the functionality of the design before the routing phase of the FPGA [9].

Fig. 7 shows a detailed schematic diagram of the elementary unit of the *ANN*. First, the neuron computes the product of its inputs, which are saved in a RAM. The corresponding synaptic weights are stored in an EEPROM and then the results are added. Finally, the obtained result is presented to the activation function unit.

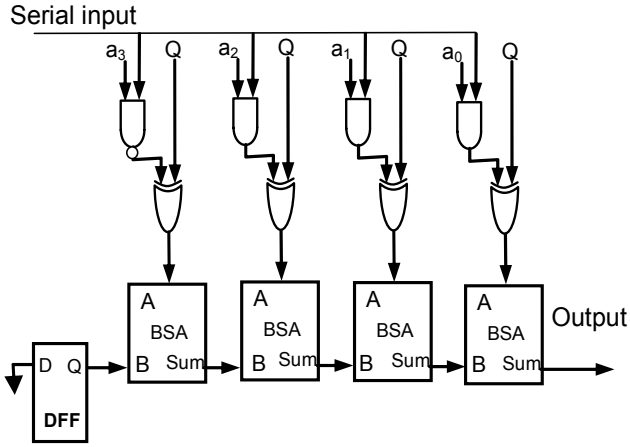

Fig. 5– A 4-bit word two's complement serial parallel multiplier (BSA denotes the bit-serial adder and a_3 is the bit position for the MSB of the parallel operand).

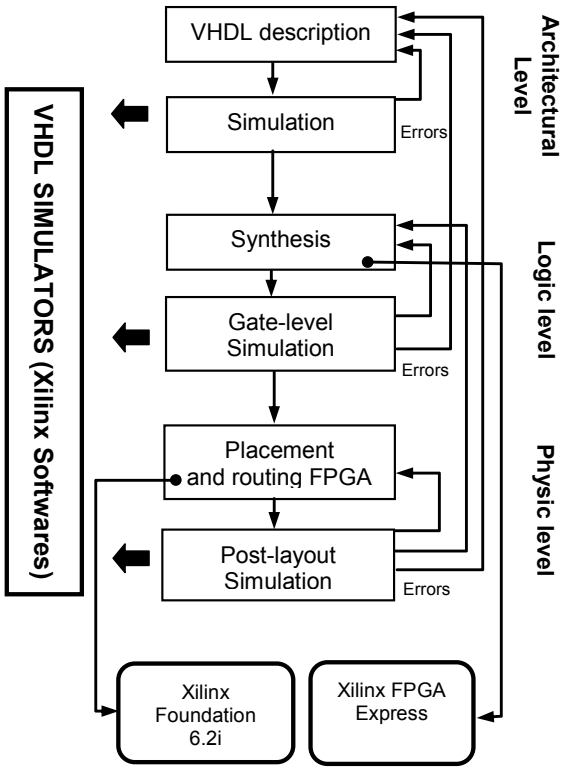

Fig. 6–Design flow.

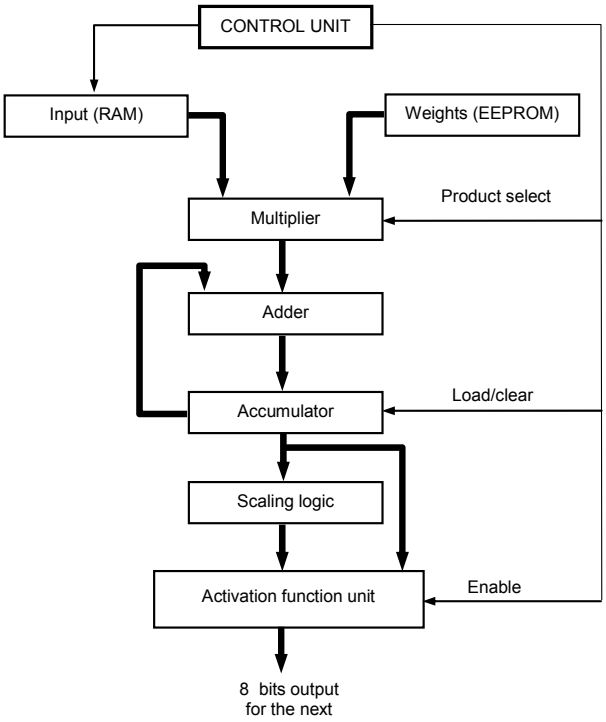

Fig. 7– Schematic diagram of a neuron.

In the same manner the structural *VHDL* description of a layer allows during the compilation phase to determine the number of neurons on this layer, which gives the possibility to synthesize layers with any number of neurons (Fig. 8).

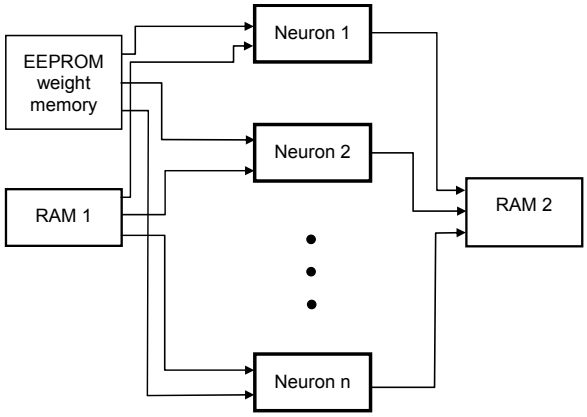

Fig. 8–Layer architecture.

5. SIMULATION AND ANALYSIS

A one input, 63 hidden neurons and 6 outputs neural network is implemented to realize the linearization and analog to digital conversion after the elaboration of the corresponding *VHDL* program. In order to test and analyze the results of simulation, it is necessary to convert the six digital outputs using a digital/analog converter. The nonlinear ADC has been tested by a sinusoidal signal to verify the capability of reproducing the nonlinear characteristic of the thermistor.

Fig.9 shows the capability of the adopted nonlinear *ANN* to reproduce the nonlinearties is evident; the done test show a difference between the reference values and those furnished by the neural model always lower than one LSB. After validation of results gotten, the final step arrives which consists on making the statistical and spectral analysis. These analysis present the interest to be able to give an appreciation on reliability and capacity of the neural nonlinear ADC to pursue signals [14], [15], [16], [17]. In brief, they determine if the synthesized network can produce in a real environment.

The test setup for a statistical analysis consists in applying a sine wave at the input of the nonlinear ADC. An histogram is built from the *N* acquisition samples. The relative number of occurrences of the distinct digital output codes is termed code density. The data are viewed in form of normalized histogram, showing the frequency of occurrence of each code from zero to full scale. Fig.10 shows the histogram obtained with taking *N*= 5000 and a sine input signal with frequency of 5kHz. Fig.11 shows the difference between the occurrence of the ideal and the neural nonlinear ADC.

No outputs zero code have been observed on the histogram which indicates that there are no missing codes. The neural model present some weak nonlinearities deduced from the shift in density from the ideal model in the histogram.

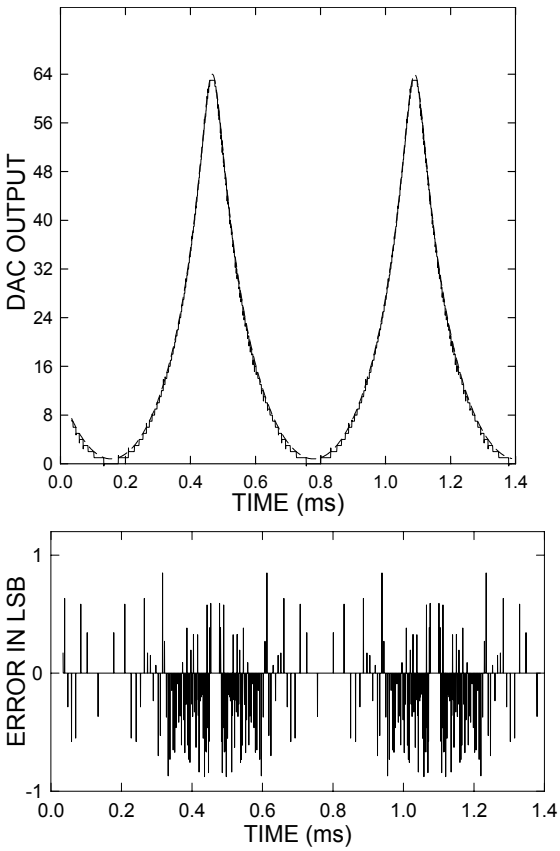

Fig . 9–Nonlinear A/D converter response (after a DAC) to a sinusoidal signal and the difference between the ideal model and the neural model.

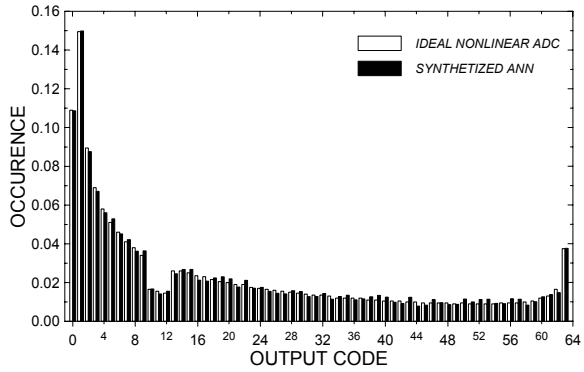

Fig. 10–Histogram of the synthesized ANN output codes.

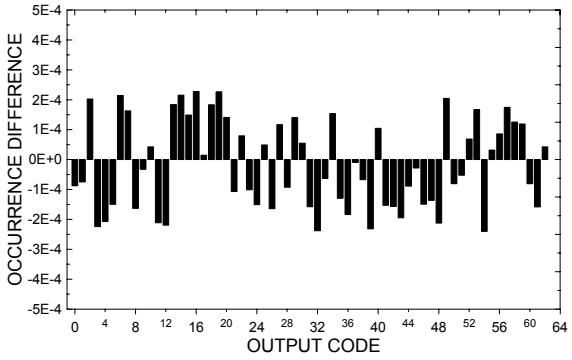

Fig. 11–Ourrence difference between the ideal nonlinear ADC and synthesized ANN.

The spectral analysis is based on the use of the Discrete Fourier Transform (DFT) applied to the output sinusoidal data (d[i]). Then the DFT gives a complex spectrum, which components are given by the equation (2).

$$D[n] = \sum_{i=0}^{N-1} d[i] e^{-j2\pi i \frac{n}{N}} \quad n = 0 \cdots N-1 \qquad (2)$$

Where N–the number of samples.

Usually, the spectral parameters of the converter under test are extracted from the normalized power spectrum ($|D[n]|^2$) in Decibels. Fig.12 shows the error between the ideal model and the neural model output spectra with taking *N*= 5000 and a sine wave input signal with frequency of 5kHz.

These tests illustrate that the corresponding output signal spectra for the ideal model and the neural model are very similar what leads to say that the characteristics of the two models are practically the same.

6. CONCLUSION

In this paper, a nonlinear analog to digital converter which is based on using artificial neural network is described. This later is based initially on the use of one neural network for each bit and after the analysis of the weight file, a new optimal architecture is deduced where all the hidden layers of the six outputs are included in the hidden layer of the LSB one. Only 63 neurons are needed in the hidden layer of the whole synthesized *ANN*.

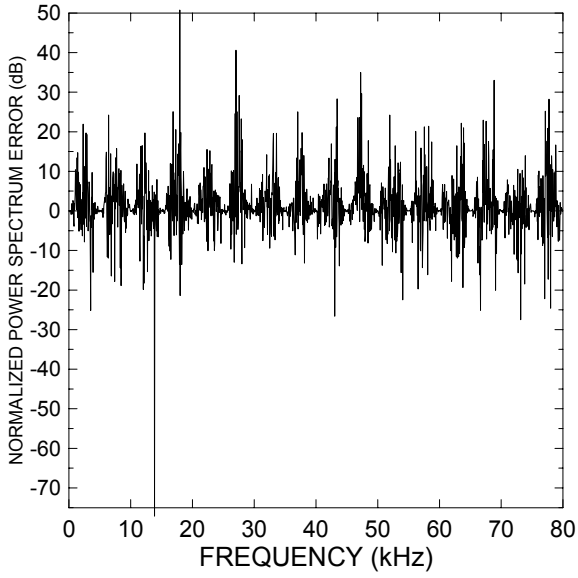

Fig. 12–Error between Ideal model and neural model output signal spectra.

Simulation results have shown the effectiveness on using neuron components in designing nonlinear A/D converter especially when the output signal of a sensor is nonlinear against the input physical variable (eg : temperature for instance). The proposed *ANN* was optimized in view of FPGA implementation. A *VHDL* program and FPGA implementation were elaborated.

The temporal, statistical and spectral analysis were carried out to show the effectiveness, the precision and the aptitude of the synthesized nonlinear ADC. This architecture based on FPGA could be expanded to realize others nonlinear ANNs applications. In this paper, reconfigurability and adaptability were the main features of the hardware implementation. For furthers nonlinear applications based sensor correction only the weights, biases, and scaling parameters are needed for reconfiguring the CLBs without changing the basic design architecture.

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Mr. Bouhedda is working on the development of intelligent instruments using artificial neural networks and fuzzy logic techniques, FPGA-implementation and ADC modeling.

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