computing@tanet.edu.te.ua
www.tanet.edu.te.ua/computing

ISSN 1727-6209
International Scientific
Journal of Computing

TESTING AND DIAGNOSIS OF DISTRIBUTED DIGITAL SYSTEMS

Vladimir Hahanov, Vladimir Yeliseev, Alexander Parfenty

Kharkov National University of Radio Electronics, 14 ave Lenin, 61166 Kharkiv, Ukraine
hahanov@kture.kharkov.ua

Abstract: *The complex system can be represented as hierarchy of simpler components. On the one hand different levels of hierarchy have an advantage for more deeply research of properties of the complex system. On the other hand a flexible model and method of testing and diagnosing of the complex system need to be developed. Moreover, international IEEE testability standards should be applied.The research presented in the current paper offers approach of testing of complex digital system based on hierarchy scaling during diagnosis experiment. Several models of testing are proposed. Main principles of testing system organization are given. The result of the work is significant time reduction of test and diagnostic of system overall.*

Keywords: *Network on Chip, System on chip, digital board, crate, testability standards, IP-Core, Integrated circuit, ARM processor.*

1. ACTUALITY OF THE RESEARCH

Modern micro- and nanotechnologies give the possibility to create Systems on Chip (SoC) and Networks on Chip (NoC) with following properties: high frequency of synchronization and performance, low power consumption, low geometries, high scale integration [1]-[4]. The components of NoCs unlike SoCs have additional possibility to interchange information using standard network protocols.

Nowadays all complex digital devices are regarded on different levels of hierarchy. The lowest level of consideration consists of modern Integrated Circuits (IC), like PLD and ASIC, in which SoCs or NoCs, triggers, and processors are implemented. The next level is formed by digital devices assembled as a single system on a board, where low level ICs represent the elements.

The sets of boards, that generate a system on crate, are the next level Personal computer IBM is a typical representation of such systems. The next level combines sets of crates or boxes into complex control system of manufacturing processes or critical technologies (aviation, airspace, nuclear-power engineering, meteorology, defense, ecology, etc.) [5]. A geographically distributed system, e.g. Internet, can be regarded as the next level of consideration.

We examine the levels of hierarchy described above with aim to construct a model and method for digital system testing with pre-defined diagnosis depth.

Reducing of time of testing and diagnosis for complex digital systems is the goal of the presented work. A general model of organization and execution of diagnostic experiment, that includes conditional and unconditional algorithms of searching of defects and is conditioned of IEEE testability standards, is the base of the research. The following three tasks are regarded to achieve the delivered goal:

1) Reviewing of testability standards;

2) Developing hierarchical model of organization and execution of diagnostic experiment that conditioned of using testability standards;

3) Building of ad hoc testing models directed towards specification of digital design description.

The digital system described on several levels of hierarchy and designed using testability standards is the object of the research. A program-technical complex F is considered as the object of testing:

$$F =< C,B,P,M >$$

where $C = \{C_1, C_2, ..., C_n\}$ – finite nonempty set of crates in system, $B = \{B_1, B_2, ..., B_m\}$ – set of boards in crate, $P = \{P_1, P_2, ..., P_k\}$ – packages on board, $M = \{m_1, m_2, ..., m_l\}$ – set of IP modules in IC. The main equation of diagnosis for the concerned object of the research is:

$$D = R \wedge L = (R_m \oplus R_r) \wedge L =$$
$$= [(T \oplus F) \oplus (T \oplus F_r)] \wedge L$$

where parameters $D, L, R, R_m, R_r, T, F, F_r$ – are: a set of detected faults in system; fault coverage; a binary Vector of Experimental Validation (VEV) that equal to number of observed outputs; a reference vector of output states; a vector of experimental validation of output states; a test; a reference device model; a real device.

Graph theory, discrete mathematics, technical diagnostics, digital systems theory, digital simulation tools are methods of the research.

2. FUNCTIONALITIES OF IEEE STANDARDS

Manufacturing of yield ratio, time-to-market design and operational reliability are three parameters that determine the efficiency of testing tools. Clearly revolutionary transformations in nano- and submicron technologies of a chip manufacturing and also for SoCs and NoCs creation send new challenges to testing and diagnosis of complex digital systems and networks [6], and [7]. Reducing of the number of rejects DL as a solution of problems mentioned above tightly connects with quality of testing [8]: $DL = 1 - Y^{(1-T)}$. Yield ratio is maximal if test covers of 100% of defects; it means luck of rejects on the market. The time of verification and testing governs by quality of the test is also an important criterion at time time-to-market. The reliability of the device depends on the fault coverage of quality of the test since the defect tested lately can lead catastrophic effects. IEEE standards [8]-[11] are world experience of the design for testability uses of leading corporations.

IEEE 1149.1-2001 Standard Test Access Port and Boundary-Scan Architecture defines of architecture and functions of test logic. It is can be embedded into the IC to provide standard approaches of testing the interconnections between ICs, testing of integrated circuits, observing or modifying of circuit activity. The test logic consists of a Boundary Scan register (BSr) with other building blocks and a Test Access Port (TAP). The problem of testing of digital device, which consists of several interconnected integrated circuits, demands of solving of following tasks: 1) checking of functionality of each component; 2) checking of proper interconnect; 3) checking of overall system functionality.

IEEE 1149.4-1999 Standard for a Mixed-Signal Test Bus [9] defines test features and test protocols of analog-digital components for testing of interconnections, breakages, short circuits, and time parameters, digital and analog characteristics.

IEEE 1149.6-2003 Standard for Boundary-Scan Testing of Advanced Digital Networks [10] extends of IEEE Std. 1149.1 with aim to standardize the Boundary-Scan structures and methods required to ensure simple, robust, and minimally intrusive Boundary-Scan testing of advanced digital networks.

Standardization of access interface to test embedded cores is the main function of the IEEE 1500 Standard for Embedded Core Test (SECT) [11]. The standard provides circuitry to access internal cores to stimulate inputs and observe outputs. Here are two approaches to check operability of the device: using Automated Test Equipment and using Built-in Self Test. In both cases it is necessary to apply test samples to inputs of the core and to propagate responses to outputs the system for further analysis. Access mechanism provides this functionality.

IEEE 1500 SECT includes two parts: hardware and Core Test Language. Main advantage of testability standards is possibility to scan internal signals of system-on-chip or system-on-board, including signals of functional units-on-chip. Interface of IEEE 1500 SECT is depicted on the Fig.1.

All components are connected to TAP-controller and tested as independent circuit, which have separate test, TAP-controller, command register, boundary scan register and command decoder. Main component of boundary scan register is scan cell, as shown on the Fig. 2. It is can be considered as hardware redundancy for each line under observation and control. The number of lines is limited in the design.

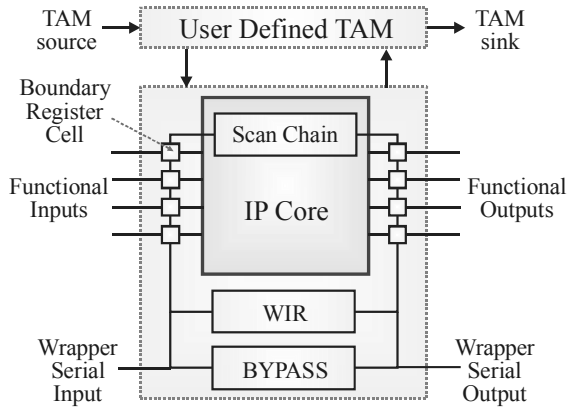

Fig. 1 – Standard IEEE P1500 Wrapper Components.

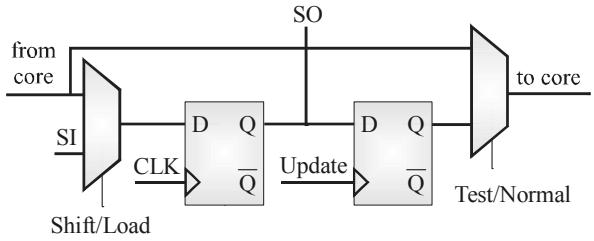

Fig. 2 – Boundary Scan Cell.

Note the time consumption is related to the work of BSr. The more register bits *L(R)* it has the more considerable testing time is. It is depends on inputs number *N(X)* and test length *L(T)*. It can be defined as $Q = N(X) \times L(T) + L(R) \times L(T)$.

3. AD HOC TECHNOLOGIES OF DIGITAL SYSTEM TESTING

Other important extension of IEEE Boundary Scan standard [8] with aim to minimize time of IP-cores testing is proposed in [12]. Each IP-core has BIST that generates pseudorandom test sequence is the main idea. All IP-cores can be tested simultaneously. Idle periods are added to the test schedule in order to avoid the test conflicts between the deterministic tests of different cores. The Advanced Microcontroller Bus Architecture (AMBA) bus is used to test distribution. Authors have proposed the methodology of optimal combination (in the view of time cost) of pseudorandom and deterministic tests for system that consists of multi-cores. The described standards is a basic instrument that can be extended by ad hoc technologies to solve more complex tasks of test synthesis, verification and diagnostics, fault simulation. The specialized technologies for the test of complex digital system that allow developing of hybrid methodology [13],[14] and combining IEEE standards with heuristics will be proposed.

On the Fig.3 the test system uses the bus for transportation of test sequences from test processor to reactions of unit-under-test and back, is presented.

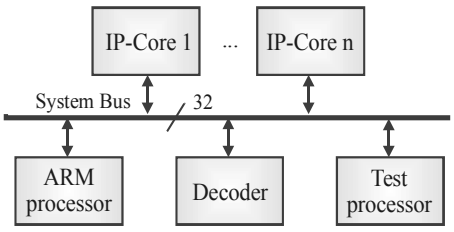

Fig. 3 – Bus architecture for digital system testing.

Use a decoder of such architecture gives the possibility to test of several IP-cores or ICs, and ARM processor also. Generating of pre-tests and patterns for all modules in digital system is a preparation of diagnostic experiment. Test, patterns and algorithms of defect searching as the diagnostic software is stored in the test processor. During of the test execution the ARM processor delivers a control to the test processor with interruption of main functions of digital system. Simplicity of configuration, possibility of diagnosis to IC and high performance are advantages of the system. High performance is defined by clock frequency and bus width:

$$\varphi = \frac{k_t \times n_t}{f \times r}, \qquad (1)$$

where k_t, n_t, f, r – the number of rows and columns (dimension) of test, clock frequency and data transfer bus width respectively.

The disadvantage of the presented architecture is impossibility of defect location and identification inside the IC.

The structure on the Fig.4 combines advantages of data transfer bus organization between IP-cores with high diagnosis depth, as in IEEE 1149 standard, is proposed to overcome the disadvantage described above.

Significant slowing of test experiment with duration defined as:

$$\varphi = \frac{k_t \times n_t}{f \times r \times L_{bsr}}, \qquad (2)$$

where L_{bsr} – length of boundary scan chain of IP-core under test, is the retribution of test quality. The proposed approach is oriented on functional testing of system components, and does not consider interconnections between IP-cores.

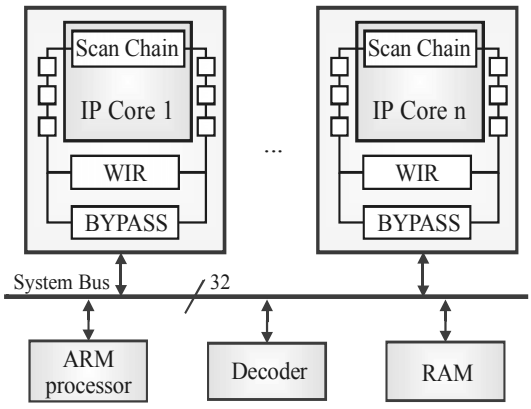

Fig. 4 - Bus architecture and Boundary Scan standard

The next architecture (Fig. 5) combines advantages of bus organization, Boundary Scan standard and BIST tools. It gives significant reducing of test experiment execution time for high defect diagnosis depth within single system component:

$$\varphi = \frac{\eta(k_t \times n_t)}{f \times r \times L_{bsr}}, \qquad (4)$$

where η – coefficient, which taking into account the part of deterministic test in whole test sequence length (plus pseudorandom sequences) for IP-core testing.

Clearly, that for verification of all digital system components with aim to diagnose it, N-number experiments need to be done.

Fig. 6 demonstrates the general structure of testing process of complex hierarchical digital system constructed with aim to check operability and locate and identify defect.

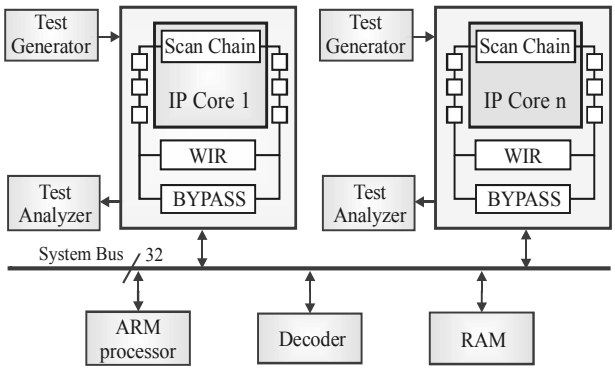

Fig. 5 – Bus architecture, BIST and Boundary Scan standard.

The several principles of testing system organization can be marked out:

1) Using of the most appropriate IEEE standards [8]-[11] for verification of components on the current level of hierarchy;

2) Determining of given depth diagnosis automatically, without using of conditional defect finding algorithms;

3) Diagnosis is running only if one component is faulty;

4) The testing procedure after repair begins from the top level to low level of hierarchy – descending diagnosis;

5) The testing procedure can start from any level of hierarchy and can finish on the level desired by engineer.

The test processor regulates of feeding of input sequences in necessary format with defined properties for specific components of considered level of hierarchy $\{C,B,P,M\} \in F$. Each component has a standard of test for checking and diagnosis of custom defects. The test process supports of automatic mode of searching of defects with the highest diagnosis depth, up to gate level or piece of source code. Process can be finished on reaching of defined diagnosis depth by the request of user. The diagnosis procedure after repair starts from the top level of organization of diagnosis experiment.

Input data are state bits of BSr, which are formed into response table $T = [T_{tr}], t = \overline{1,p}; r = \overline{1,q+n}$, with dimension $p \times n$, p – number of test vectors, n – number of BSr bits.

(BP – repair; $D+$ – user is satisfied with diagnosis depth).

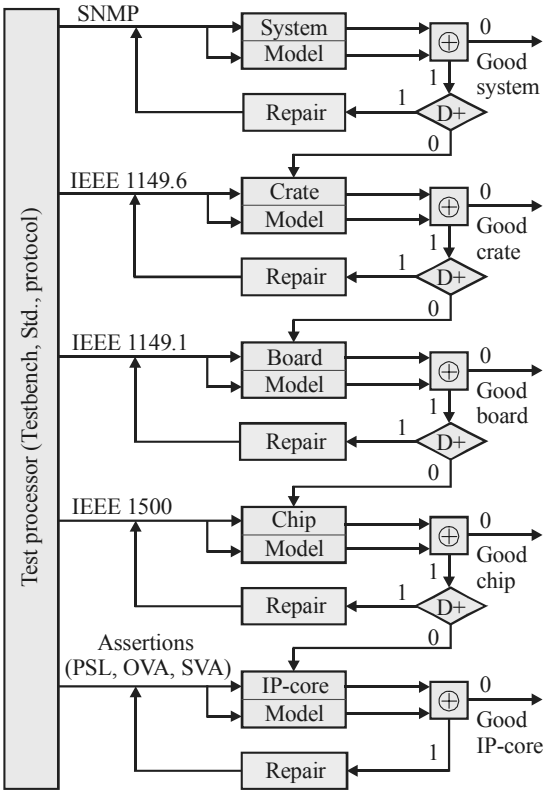

Fig. 6 – Structure of complex digital system testing process.

The Experimental Check Vector (ECV) $Y = (Y_1, Y_2, ..., Y_i, ..., Y_n)$ is the result of each test-vector from response table. ECV allows identification and localization of fault by using of the following equations:

$$D^s = \left(\bigcap_{\forall i(Y_i=1)} D_i\right) \setminus \left(\bigcup_{\forall i(Y_i=0)} D_i\right);$$
$$D^m = \left(\bigcup_{\forall i(Y_i=1)} D_i\right) \setminus \left(\bigcup_{\forall i(Y_i=0)} D_i\right); \quad (5)$$

where $(D_i, D^s; D^m)$ – respectively: faults, which behavior is described using predicate $Y_i = L_i(X_i)$; set of single faults, detected by test-vector; set of multiple faults, defined by the second equation.

Equations (5) give the possibility of significant rising of diagnostics depth in case of all faults and possible incorrectness were covered during assertion definition. For example, there is assertion system, forming following fault coverage table D_i:

D_1	D_2	D_3	D_4	Y^1	Y^2
1	.	1	1	1	1
.	1	1	.	1	1
1	1	.	.	0	1
.	1	.	1	0	0

(6)

Application of the first equation of (10) for vector Y^1 gives the results:

$$D^s = [(D_1 \cup D_3 \cup D_4) \cap (D_2 \cup D_3)] \setminus$$
$$\setminus [(D_1 \cup D_2) \cup (D_2 \cup D_4)] = D_3$$

which allows to exclude faults D_1, D_2, D_4 from suspected ones list. If it is considered presence of multiple faults in design then it is necessary to use second equation from (5) for (116 because the first one doesn't detect faults at all:

$$D^m = [(D_1 \cup D_3 \cup D_4) \cup (D_2 \cup D_3) \cap$$
$$\cap (D_1 \cup D_2)] \setminus [(D_2 \cup D_4)] = (D_1 \cup D_3)$$

The proposed approach gives possibility to detect single fault, and at least one of the multiple, existing in list D^m.

4. CONCLUSIONS

International IEEE standards developed for testing and diagnosis of program-technical complexes and broad range of electronic system: starting with components inside IC, ending with complex systems, consisting of boards and crates were viewed in the presented research. The IEEE standards 1149.1, 1149.4, 1149.6 and 1500 demonstrate wide resource for solving the following tasks: component functional testing; interconnection testing; system on board functional testing; system on crate functional testing.

Analog components; digital components; mixed components; discrete elements; printed circuit boards, consisted of mentioned components are the objects of testing. We consider the block-hierarchical method of testing and diagnosis: the complex system is represented as hierarchy of simpler components.

Combination of ad hoc technologies with existed testability standards and with specialized schematic solutions give the possibility of reducing the time of testing and diagnosis of complex digital systems in a few times. The described strategy can be regarded as the main innovation in the presented work.

Practical application of the current research is applying the new model of diagnosis process model to design of complex hierarchical digital systems that are operated the critical technologies.

Future works are connected with reached results will be oriented to implementations developed model for testing and diagnosis complex control systems of for critical technologies of nuclear power stations.

Concerning the new System JTAG [15] appearance in the EDA world market the next step of improving suggested diagnosis technology is connected with systems wrapping development based on mentioned draft standard.

5. REFERENCES

[1] Grant Martin. *The Reuse of Complex Architectures*. IEEE Design and Test of Computers. November-December 2002. P. 4-6.

[2] Rajesh K. Gupta and Yervant Zorian. *Introducing Core-Based System Design. IEEE Design & Test of Computers*. November-December 1997. P. 15-25.

[3] Yervant Zorian. What is Infrastructure IP? IEEE *Design & Test of Computers*. May-June 2002. P. 5-7.

[4] L. Benini and G. D. Micheli. *Networks on chips: A new soc paradigm*. IEEE Computer. Vol. 35. No. 1. 2002. P. 70–78.

[5] Yeliseev V.V., Largin V.A., Pivovarov G.Yu. *Programmno-tehnicheskie kompleksy ASU TP*. K.: IPC "Kievskiy universitet". 2003. P. 429 (In Russian).

[6] Yervant Zorian. *Advances in Infrastructure IP*. IEEE Design & Test of Computers. May-June 2003. P. 49-56.

[7] Yervant Zorian. *Test Requirements for Embedded Core-Based Systems and IEEE P1500*. In Proceedings IEEE International Test Conference (ITC). Washington, DC. November 1997. IEEE Computer Society Press. P. 191-199.

[8] Abramovici M., Breuer M.A. and Friedman A.D. *Digital systems testing and testable design*. Computer Science Press. 1998. 652 p.

[9] IEEE STD 1149.1-2001. *Standard Test Access Port and Boundary-Scan Architecture*. New York. 2001. 208 p.

[10] IEEE STD 1149.4-1999. *IEEE Standard for a Mixed-Signal Test Bus*. New York, 2000. 84 p.

[11] IEEE STD 1149.6-2003. *Standard for Boundary-Scan Testing of Advanced Digital Networks*. New York. 2003. 139 p.

[12] IEEE P1500/D11. January 2005. *Draft Standard Testability Method for Embedded Core-based Integrated Circuits*. New York. 2005. 138 p.

[13] Gert Jervan, Petru Eles, Zebo Peng, Raimund Ubar, Maksim Jenihhin. *Test Time Minimization for Hybrid BIST of Core-Based Systems*. Proceedings of the 12th Asian Test Symposium (ATS'03). P.318-323.

[14] C. A. Papachristou, F. Martin, and M. Nourani. *Microprocessor based testing for core-based system on chip*. In Proceedings of the 36th ACM/IEEE conference on Design automation conference. ACM Press. 1999. 586-591 p.

[15] System JTAG. Supporting eXternal and Embedded Boundary Scan Test (XBST, EBST). A white paper from the SJTAG Core Group. Version 0.4.1. November 2005. 29 p.

Vladimir Ivanovich Hahanov, *Doctor of Tech. Science, professor of KNURE. Dean of Computer Engineering Faculty. Scientific interests: digital systems and networks design and diagnosis. Address: Ukraine, 61166, Kharkov, Lenin 14, ave, tel. (+380)-57-7021326. E-mail: hahanov@kture.kharkov.ua*

Vladimir Vasilievich Yeliseev, *closed (joint-stock) company «North Donetsk scientific production association "Impuls"», North Donetsk Institute of East Ukrainian National University. Director of closed (joint-stock) company «Impuls», PhD of NDTI EUNU*

Alexander Nikolaevich Parfentiy, *PhD student of KNURE. Scientific interests: digital systems and networks design and diagnosis. Address: Ukraine, 61166, Kharkov, Lenin 14, ave, tel. (+380)-57-7021326.*