Date of publication DEC-31, 2021, date of current version JUL-07, 2021.
www.computingonline.net / computing@computingonline.net

Print ISSN 1727-6209
Online ISSN 2312-5381
DOI 10.47839/ijc.20.4.2447

The Parametric Optimization of Voltage Multiplier

VOLODYMYR SAMOTYY[1], ULYANA DZELENDZYAK[2], ANDRIY PAVELCHAK[3]

1) Department of Automatic Control and Information Technology, Cracow University of Technology, Warszawska 24, Cracow, 31155, Poland, (e-mail: vsamotyy@pk.edu.pl)
2) Department of Computerized Automatic Systems, Lviv Polytechnic National University, S. Bandery 12, Lviv, 79013, (e-mail: u.dzelendzyak@gmail.com)
3) Department of Computerized Automatic Systems, Lviv Polytechnic National University, S. Bandery 12, Lviv, 79013, (e-mail: apavelchak@gmail.com)

Corresponding author: Volodymyr Samotyy (e-mail: vsamotyy@pk.edu.pl).

ABSTRACT The evolutionary model of voltage multiplier parametric optimization which includes 5 diodes and 5 capacitors is reviewed. It executes the transformation of alternating into constant voltage using a five times larger amplitude. The valve work is modelled according to the scheme of an ideal key. The original mathematical model of voltage multiplier which includes additional logical variables is deducted. It accepts binary meanings 0 and 1, where 0 corresponds to closed valve status and 1 corresponds to open. In order to receive such a model, it is necessary to indicate the amount of open and closed valve combinations. Then for each of them, it is necessary to write the system of differential equations. Comparing them with each other the single differential equation system with additional logical variables is written as a generalization. The evolutional model is used in order to select the capacitor volume meaning. The goal function forecasts two conditions: maximum meaning of output voltage 1 kV and its minimal fluctuations in the stable regime.

KEYWORDS evolutionary model; parametric optimization; ideal key; voltage multiplier; logical variables.

I. INTRODUCTION

TASKS in which voltage transformation needs to be executed are widespread in practice. The frequency and amplitude are the voltage parameters. Devices that execute two transformations at the same time already exist, providing the transformation of AC voltage into a constant increasing amplitude of output voltage, by devices known as voltage multipliers. The amplitude multiplication is executed using cyclic charging of capacitors. To investigate the work dynamic of such devices a mathematical model must be created. After completing the numerical integration of these equations during a preset time interval, the calculation of the transition process can be executed. If the integration is executed over a significant amount of time, a stable regime will be obtained. The investigated multiplier includes 5 diodes, so the mathematical model should be chosen accordingly. The model of an ideal key, which is simple in realization and has satisfactory precision, has been chosen. If the diodes have been modeled using the ideal key scheme, the changeable structure of an electric circle can be received. Our model includes the existence of additional logical variables in the dynamic equation. These take values of 0 or ±1 depending on the diodes condition. The additional logical variables change their values depending on the open and closed valves conditions.

II. ANALYSIS OF PUBLICATIONS

Electronic devices require DC voltage sources. So, in a large amount of scientific works DC voltage sources were investigated. For example, in [1-3] the electronic converter dynamic properties were analyzed in a specific usage but there is no analysis of the influence of the parameters on the converter work dynamic. In [4-8] a DC voltage rectifier with a triple band was proposed. In comparison with other similar constructions, it is highly efficient and compact. The analysis of an active transistor rectifier for railway transport was

reviewed in [9]. In this device the three-phase voltage is rectified and then turned into alternating voltage of another frequency. The result of this development is confirmed by experimental data. In [10] a transformer with several regulated voltages at the input was reviewed. For this transformer with several output signals, parametric optimization needs to be executed. The active topology of a three-phase rectifier was described in [11-14]. The proposed topology is tested experimentally. It is characterized by less power loss during unbalanced loads. The mild thyristors switch in inverters was described in [15]. In the proposed scheme, a marginal overload connected with the discharge capacitor was offered. A DC voltage transformer used to convert to DC voltage of another amplitude (converter) in a field transistor was described in [16]. The well-known parallel invertor scheme supplemented by an additional transformer is used. The disadvantage is the absence of a mathematical model for dynamic characteristic analyses. A four-cell voltage multiplier was reviewed in [17-19]. The proposed scheme includes 10 thyristors and 5 capacitors. To receive a high voltage at the input, resonance is used. In this work experimental charts are used, but the dynamic equations that describe the work of this multiplier are absent. A convertor with a voltage multiplier was described in [20, 21]. All the description reflects the advantages of the proposed scheme. To calculate the frequency, inductance and amplitude of the output voltage, several formulas are used. The large amount of experimental results gives an opportunity to understand the dynamic processes in the convertors. The disadvantage is the absence of dynamic equations and the conditions of the diodes switch. The problems of parametric optimization were described in [22], where the analysis of a DC voltage motor system's dynamics was performed. To sum up the literature review we may admit that an appropriate mathematical model does not exist. That is why, there no publications on parametric five-cell voltage multipliers. This conclusion unquestioningly confirms the relevance of this article.

III. THE DYNAMICS EQUATION OF THE FIVE-CELL VOLTAGE MULTIPLIER

A converter of DC into AC with five time amplitudes multiplied at the same time is reviewed. It should be noticed that such transformation is possible when the capacity has a great resistance (several kΩ). The principal scheme of this transformer is shown in Fig. 1. It includes a transformer (Tr), 5 diodes (D_1, D_2, D_3, D_4, D_5) and 5 capacitors (C_1, C_2, C_3, C_4, C_5) and capacity (r_L). The cyclic capacitors charge is executed by thyristors switching. On the C_1 capacitor single voltage is accrued and on the others double voltage is accrued. So, when the resistance of charge is connected to capacitors C_1, C_3, C_5 a voltage multiplied by 5 will be received.

In order to create mathematical models of the multipliers voltage, the appropriate algorithm is created. The first step is the analysis of the number of combined open and closed valves. Then each combination is described by a differential equation system. The additional logical variables k_i, $i = 1$, 2, ... which take values of 0, 1, are introduced. Usually the number of these is the same as the number of valves. The value 0 corresponds to closed valve status and 1 means open valve status. Further, it is necessary to compare the equations obtained for separate combinations and generalize these using variables k_i. The state equation should be added by the open and closed valves conditions, in which variables k_i. take values of 0 and 1. Fig. 1 represents the scheme of the five-cell voltage multiplier.

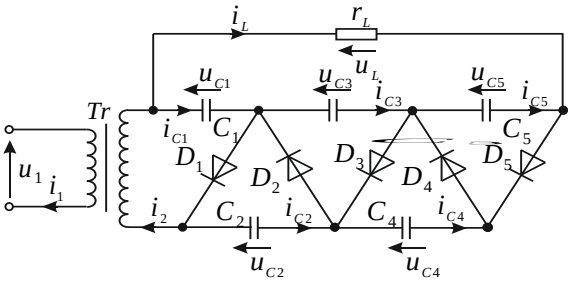

Figure 1. Basic diagram of five-cell voltage multiplier

Analyzing the work of the multiplier, we come to the conclusion that in this scheme more than 1 diode cannot be open at the same time. But the situation could exist when all valves are closed. So, we have six combinations of open and closed valves: 1) all 5 valves are closed; 2) D_1 is open and the rest are closed; 3) D_2 is open and the rest are closed; 4) D_3 is open and the rest are closed; 5) D_4 is open and the rest are closed; 6) D_5 is open and the rest are closed.

The first combination (Fig. 2) is characterized by the following conditions:

$$i_2 = i_{C2} = i_{C4} = 0, \quad (1)$$

$$i_{C1} = i_{C3} = i_{C5} = -i_L, \quad (2)$$

$$i_L = (u_{C1} + u_{C3} + u_{C5}) / r_L, \quad (3)$$

where i_{Cj}, $j = 1, 2, ..., 5$ – capacitor currents;

u_{Cj}, $j = 1, 2, ..., 5$ – voltages on capacitors;

i_L, r_L – current and load resistance,

i_2 – the secondary winding current transformer.

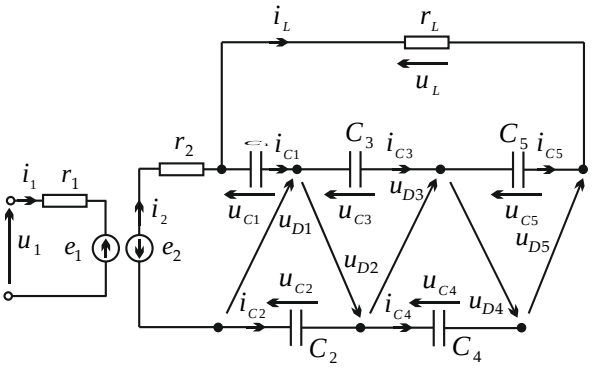

Figure 2. The first combination

Taking into account these conditions, the differential equations of the capacitors can be written as follows:

$$\frac{du_{C2}}{dt} = \frac{du_{C4}}{dt} = 0, \tag{4}$$

$$\frac{du_{C1}}{dt} = -\frac{i_L}{C_1}, \ \frac{du_{C3}}{dt} = -\frac{i_L}{C_3}, \ \frac{du_{C5}}{dt} = -\frac{i_L}{C_5}, \tag{5}$$

where C_j, $j = 1, 2, ..., 5$ – capacitors' receptivity.

For this combination, the transformer is not loaded, so it is described only by one equation:

$$\frac{d\psi}{dt} = g_1(u_1 - r_1 i_1), \ g_1 = \alpha_1 / (\alpha'' + \alpha_1), \tag{6}$$

where ψ is the main transformer's flux linkage; u_1, i_1, r_1 – voltage, current and the resistance of the primary winding of the transformer; α_1 – the value inverse to the scattering inductance of the primary winding of the transformer; α'' – the inverse differential inductance of the transformer, which is determined by the magnetization curve $\varphi(\psi)$.

The second combination (Fig. 3) is characterized by conditions:

$$i_2 - i_{C1} - i_L = 0, \ i_{C2} = i_{C4} = 0, \tag{7}$$

$$i_{C3} = i_{C5} = -i_L, \tag{8}$$

$$i_L = (u_{C1} + u_{C3} + u_{C5}) / r_L, \tag{9}$$

The capacitors equations will remain unchanged and Eq. (5) will now take the form

$$\frac{du_{C1}}{dt} = \frac{i_2 - i_L}{C_1}, \ \frac{du_{C3}}{dt} = -\frac{i_L}{C_3}, \ \frac{du_{C5}}{dt} = -\frac{i_L}{C_5}, \tag{10}$$

The transformer is described by two equations:

$$\frac{d\psi}{dt} = g_1(u_1 - r_1 i_1) + g_2(-u_{C1} - r_2 i_2), \tag{11}$$

$$\frac{di_2}{dt} = a_1(u_1 - r_1 i_1) + a_2(-u_{C1} - r_2 i_2), \tag{12}$$

where r_2 is the resistance of the secondary winding of the transformer; α_2 – the value inverse to the scattering inductance of the secondary winding of the transformer; $g_1 = \alpha_1 / g$, $g_2 = \alpha_2 / g$, $g = \alpha'' + \alpha_1 + \alpha_2$, $a_1 = -\alpha_2 g_1$, $a_2 = \alpha_2(1 - g_2)$.

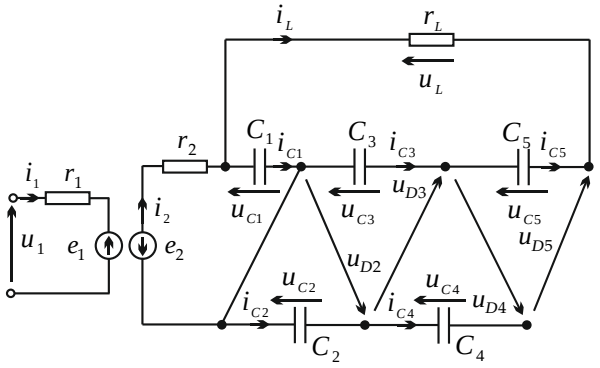

Figure 3. The second combination

Similarly, it is possible to write the dynamics equation of the remaining four combinations. Then, the six differential equations system is combined into one system for comparison. This is achieved using the additional logical variables k_1, k_2, k_3, k_4, k_5, which simulate the operation of diodes D_1, D_2, D_3, D_4, D_5. The logical variables k_i takes value 0 when diode D_i is closed and 1 when D_i is opened. To sum up all the variants of diodes switching, a common equations system will be used. This should be written in matrix form:

$$\frac{dX}{dt} = BZ(t), \tag{13}$$

where $X = (\psi, i_2, u_{C1}, u_{C2}, u_{C3}, u_{C4}, u_{C5})^T$ -variables state vector; $B = diag(D, C^{-1})$ – coefficient matrix; $Z(t) = (E, I_C)^T$ – time functions vector.

The introduced denotations can be described as below:

$$D = \begin{bmatrix} g_1 & g_2 \\ a_1 & a_2 \end{bmatrix}; \tag{14}$$

$$\left.\begin{aligned} g_1 &= \alpha_1 / g,\ g_2 = k_{15}\alpha_2 / g, \\ g &= \alpha'' + \alpha_1 + k_{15}\alpha_2, \end{aligned}\right\} \quad (15)$$

$$a_1 = -k_{15}\alpha_2 g_1,\ a_2 = k_{15}\alpha_2(1-g_2), \quad (16)$$

$$C = \mathrm{diag}(C_1, C_2, C_3, C_4, C_5), \quad (17)$$

$$E = (u_1 - r_1 i_1,\ U_C - r_2 i_2)^T, \quad (18)$$

$$U_C = -u_{C1} + \sum_{i=2}^{4} (-1)^i k_{i5} u_{Ci} - k_5 u_{C5}, \quad (19)$$

$$I_C = (i_{C1}, i_{C2}, i_{C3}, i_{C4}, i_{C5})^T, \quad (20)$$

$$i_{C1} = i_2 - i_L,\ i_{C2} = (k_1 - 1) i_2,\ i_{C3} = k_{12} i_2 - i_L, \quad (21)$$

$$i_{C4} = -k_{13} i_2,\ i_{C5} = k_{14} i_2 - i_L, \quad (22)$$

$$i_L = (u_{C1} + u_{C3} + u_{C5}) / r_L, \quad (23)$$

$$\left.\begin{aligned} k_{15} &= \sum_{i=1}^{5} k_i,\ k_{25} = \sum_{i=2}^{5} k_i, \\ k_{35} &= \sum_{i=3}^{5} k_i,\ k_{45} = k_4 + k_5. \end{aligned}\right\} \quad (24)$$

The conditions of valves closing are as follows:

$$\text{if } ((k_1 == 1) \text{ and } (i_2 < 0)) \text{ then } k_1 = 0, \quad (25)$$

$$\text{if } ((k_2 == 1) \text{ and } (i_2 > 0)) \text{ then } k_2 = 0, \quad (26)$$

$$\text{if } ((k_3 == 1) \text{ and } (i_2 < 0)) \text{ then } k_3 = 0, \quad (27)$$

$$\text{if } ((k_4 == 1) \text{ and } (i_2 > 0)) \text{ then } k_4 = 0, \quad (28)$$

$$\text{if } ((k_5 == 1) \text{ and } (i_2 < 0)) \text{ then } k_5 = 0. \quad (29)$$

The conditions of valves opening are as follows:

$$\text{if}((k_i == 0)\&\&(u_{Di} > 0)) \text{ then } k_i = 1, \quad (30)$$

$$u_{Di} = (-1)^{i+1} \sum_{j=1}^{i} (-1)^j u_{Cj} + (-1)^i \frac{d\psi}{dt},\ i = \overline{1, 5}, \quad (31)$$

where u_{Di} – voltage on the i-th valve in the closed state.

If one of the conditions (25)–(29) is met, the valve will be closed. If the condition (30) was met, the valve would be opened. It should be taken into account that condition (30) can be checked only when all the valves are closed. The conditions (25)–(29) can be checked only when one valve is open.

IV. THE PARAMETRIC OPTIMIZATION

To develop the mathematical model of the voltage multiplier a program has been written using C# language and the simulation of its dynamic processes has been executed.

The transformer feeding voltage is performed by the following equation:

$$u_1 = U_m \sin(2\pi f t), \quad (32)$$

where U_m=311 V, f=50 Hz.

The mathematical model's calculation has been executed using the following device parameters: $r_1 = r_2$=0.1 Ω; r_0=1 kΩ; α_1=100 H^{-1}; α_2=200 H^{-1}.

The magnetization curve is approximated by the following equations:

$$\varphi(\psi) = \begin{cases} m_1\psi & if\ |\psi| > \psi_1 \\ S_3(\psi) & if\ \psi_1 \le |\psi| \le \psi_2 \\ m_2\psi - m_0 & if\ |\psi| > \psi_2 \end{cases}, \quad (33)$$

where m_1=0.25 H^{-1}; m_2=3 H^{-1}; m_0=1.9 A; ψ_1=0.2 Wb; ψ_2=0.9 Wb; $\varphi(\psi_1)$=0.05 A; $\varphi(\psi_2)$=0.9 A; $S_3(\psi)$ is the cubic spline

To obtain the optimal characteristics of the voltage multiplier, the capacitor parametric optimization of $C_1 - C_5$ has been executed using the classic genetic algorithm with genes represented as real numbers [10, 11]. During the model simulation, it was discovered that the capacitor values influence the amount of output signal pulsations and its periodicity. To search for the optimum, the final area of the transitional process is used.

Integration of the model's dynamic equation is executed on the time span T=18 seconds. As a criterion for the fitness function value, the amount of output voltage pulsation is chosen at [17.5, 18] second interval. The fitness value is calculated using the following formula:

$$\begin{aligned} &Fit = u_{L\max} - u_{L\min}, \\ &\text{if } (u_{L\min} < u_m) \text{ then } Fit = Fit + u_m - u_{L\min}, \end{aligned} \quad (34)$$

where u_m=1200 V.

During calculation of the fitness value, an additional condition that provides the parameters rejection when the output signal is less than 1200 V is used.

The optimum research for the dynamic device characteristics is executed according to preset criteria for the fitness function at established capacitors values: $C_i \in [10^{-6}; 5\cdot10^{-3}]$ F, i=1, 2, ..., 5. The amplitude fluctuation does not exceed 26 V in the stable regime. The capacity of capacitors C_1, C_3, C_4, C_5 reaches the top of the limit of 5 mF. But the capacity of capasitor C_2 for the fitness value (34) is 228 μF. At the same time, the maximum value of the load voltage at the stable state is 1311 V, which is 4.2 times more than supply voltage. It is impossible to achieve the five-fold voltage multiplication because of losses on the supports. The greater the capacitance value C_1, C_3, C_4, C_5 is, the better will be the result of the voltage multiplier. This will influence the capacitance value C_2.

For the genetic algorithm the population settings of 60 chromosomes are chosen, a mutation probability within 3–15%, and a coefficient of pleasure selection of 1.7 or 1.8 is adopted. The 1 chromosome is chosen for elitism.

In the process of device model investigation, it is detected that level of the direction voltage u_L depends on the capacitor value C_2 (Fig. 4).

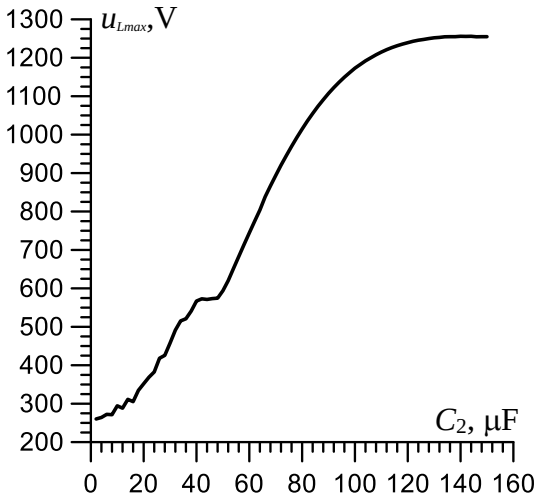

Figure 4. The dependence of maximum voltage values u_L for capacity C_2

This dependence is linear in the range from 1 mkF to 120 mkF. In the range from 160 mkF to 200 mkF, the voltage level u_L remains almost stable, therefore in Figure 4 we have limited the value C_2=160 μF. The capacitance values of the other capacitors reach the maximum possible values. So, we accepted $C_1 = C_3 = C_4 = C_5$ =5 mF. In order to ensure a stable regime, the dynamic equations are iterated at intervals of 20 sec. This fully guarantees the absence of the transitional process.

In Fig. 5 the time dependence of the load voltage for capacity C_2 = 60 μF is shown. The transitional process has an exponential character with such parameters. During the first second the voltage increases rapidly. Then there is a steady increase of voltage. It is necessary to take this fact into account because the duration of the transition process is more than 10 sec and this is quite enough as for electric circle.

In Fig. 6 shows the analogous dependence for the capacity load voltage C_2=120 μF. In this case, the transitional process is more equable and subsides twice as fast.

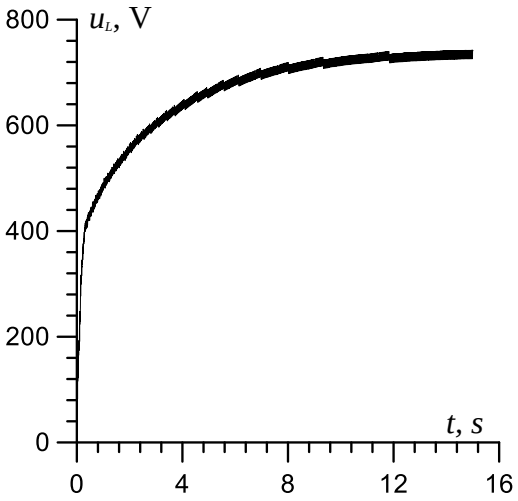

Fig. 5 – The time dependence of voltage u_L for capacity C_2=60 μF

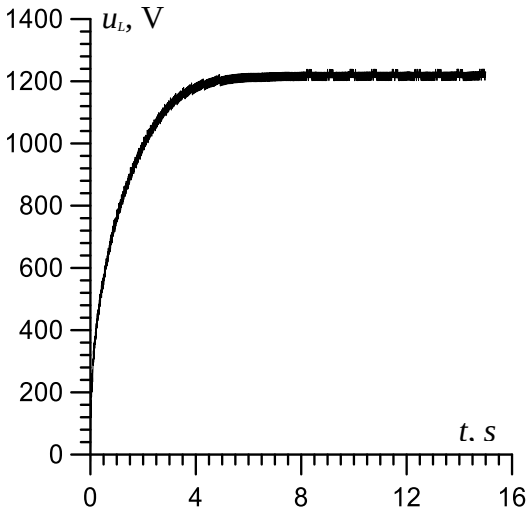

Figure 6. The time dependence of $u_L$voltage for capacity C_2=120 μF

V. CONCLUSION

In this article the mathematical model for the identification of a voltage multiplier based on five capacitors and five diodes is developed. The peculiarity of the approach is the usage of additional logical variables for modeling the working of the valves. This greatly simplifies the mathematical model and makes it suitable for explicit methods of numerical integration. For the parametric optimization analysis, a genetic algorithm is used. It is identified that the most significant impact on the final result is that of capacitor C_2 and the maximum load voltage achieved is C_2=130 μF.

References

[1] T. Suntio, J. Viinamäki, J. Jokipii, T. Messo, A. Kuperman, "Dynamic characterization of power electronic interfaces," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, pp. 949-961, 2014. https://doi.org/10.1109/JESTPE.2014.2313704.

[2] F. Harirchi, M. G. Simões, "Enhanced instantaneous power theory decomposition for power quality smart converter applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9344-9359, 2018. https://doi.org/10.1109/TPEL.2018.2791954.

[3] A. Kirubakaran, S. Jain, R. K. Nema, "DSP-controlled power electronic interface for fuel-cell-based distributed generation," *IEEE Transactions on Power Electronics*, vol. 26, pp. 3853-3864, 2011. https://doi.org/10.1109/TPEL.2011.2138162.

[4] J. Liu, X. Y. Zhang, "Compact triple-band rectifier for ambient RF energy harvesting application," *IEEE Access*, vol. 6, pp. 19018-19024, 2018. https://doi.org/10.1109/ACCESS.2018.2820143.

[5] M. A. Al-Absi, S. R. Al-Batati, "Hybrid internal Vth cancellation rectifiers for RF energy harvesting," *IEEE Access*, vol. 8, pp. 51976-51980, 2020. https://doi.org/10.1109/ACCESS.2020.2980080.

[6] L. Huang, A. Murray, B. W. Flynn, "A high-efficiency low-power rectifier for wireless power transfer systems of deep micro-implants," *IEEE Access*, vol. 8, pp. 204057-204067, 2020. https://doi.org/10.1109/ACCESS.2020.3036703.

[7] T. B. Soeiro, J. W. Kolar, "Analysis of high-efficiency three-phase two- and three-level unidirectional hybrid rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 3589-3601, 2012. https://doi.org/10.1109/TIE.2012.2205358.

[8] B. Leelachariyakul, P. Yutthagowith, "Resonant power frequency converter and application in high-voltage and partial discharge test of a voltage transformer," *Energies*, vol. 14, issue 7, 2014, 2021. https://doi.org/10.3390/en14072014.

[9] M. Fan, L. Shi, Z. Yin, Y. Li, "A novel pulse density modulation with semi-bridgeless active rectifier in inductive power transfer system for rail vehicle," *CES Transactions on Electrical Machines and Systems*, vol. 1, no. 3, pp. 397-404, 2017. https://doi.org/10.23919/TEMS.2017.8241361.

[10] G. P. Adam, I. Abdelsalam, L. Xu, J. Fletcher, G. Burt, B. Williams, "Multi-tasking DC–DC and DC–AC converters for DC voltage tapping and power control in highly meshed multi-terminal HVDC networks," *IET Power Electronics*, vol. 10, pp. 2217–2228, 2017. https://doi.org/10.1049/iet-pel.2016.1035.

[11] Y. Li, A. Junyent-Ferre, J-M. Rodriguez-Bernuz, "A three-phase active rectifier topology for bipolar DC distribution," *IEEE Transactions on Power Electronics*, vol. 33, pp. 1063-1074, 2018. https://doi.org/10.1109/TPEL.2017.2681740.

[12] T. Pajchrowski, M. Krystkowiak, D. Matecki, "Modulation variants in DC circuits of power rectifier systems with improved quality of energy conversion – Part I," *Energies*, vol. 14, issue 7, 1876, 2021. https://doi.org/10.3390/en14071876.

[13] A. Monpapassorn, "Low output impedance dual CCII full-wave rectifier," *International Journal of Electronics*, vol. 100, pp. 648-654, 2013. https://doi.org/10.1080/00207217.2012.720943.

[14] S. Xie, Y. Sun, M. Su, J. Lin, Q. Guang, "Optimal switching sequence model predictive control for three-phase Vienna rectifiers," *IET Electric Power Applications*, vol. 12, pp. 1006-1013, 2018. https://doi.org/10.1049/iet-epa.2018.0033.

[15] W. Mazgaj, B. Rozegnał, Z. Szular, "Three-phase two-level voltage source inverter with a transistor soft switching system resistant to control disruptions," *Przegląd Elektro-techniczny*, R. 92, Nr. 3, pp. 148-153, 2016.

[16] B.-R. Lin, "Hybrid full-bridge converter for DC microgrids: analysis and implementation," *IET Power Electronics*, vol. 11, pp. 817-824, 2018. https://doi.org/10.1049/iet-pel.2017.0504.

[17] A. Kawa, R. Stala, A. Mondzik, S. Pirog, A. Penczek, "High-power thyristor-based DC–DC switched-capacitor voltage multipliers: basic concept and novel derived topology with reduced number of switches," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 6797-6813, 2016. https://doi.org/10.1109/TPEL.2015.2505906.

[18] C. Nunez, J. Lira, N. Visairo, R. Echavarría, "Analysis of the boundaries to compensate voltage sag events using a single phase multi-level rectifier," *European Power Electronics and Drives*, vol. 20, pp. 5-11, 2010. https://doi.org/10.1080/09398368.2010.11463772.

[19] R. V. White, G. J. Miller, B. M. Duduman, R. W. Erickson, "Recent developments in GaAs power switching devices including device modeling," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition*, 16-20 March 2014, Fort Worth, TX, USA. https://doi.org/10.1109/APEC.2014.6803506.

[20] M. Shang and H. Wang, "LLC converter with reconfigurable voltage multiplier rectifier for high voltage and wide output range applications," Proceddings of the IECON 2017 – 43rd Annual Conference of the IEEE Industrial Electronics Society, 2017, pp. 1279-1285, https://doi.org/10.1109/IECON.2017.8216218.

[21] W. Kongnun, P. Silapan, "A single MO-CFTA based electronically/temperature insensitive current-mode half-wave and full-wave rectifiers," *Advances in Electrical and Electronic Engineering*, vol. 11, no. 4, pp. 275-283, 2013. https://doi.org/10.15598/aeee.v11i4.847.

[22] V. Samotyy, A. Pavelchak, U. Dzelendzyak, "The method selection of control system's parametric optimization," *Technical Transactions*, vol. 3–E/2016, Cracow University of Technology Press, pp. 237-249, 2016.

VOLODYMYR SAMOTYY received an M.S. in Automation from Lviv Polytechnic National University, Ukraine in 1984, a Ph.D. in 1990, and a D.S. in computers, systems and networks, elements and devices of computers and control systems in 1997. He has been a Professor since 2001. He is currently a Full Professor with the Department of Automation and Information Technologies, Cracow University of Technology, Poland, and the Department of Information Security Management, Lviv State University of Life Safety, Ukraine. His research interests include evolutionary models, numerical methods, information security, and digital signal processing. ORCID: 0000-0003-2344-2576

ULYANA DZELENDZYAK, received an M.S. in Applied Mathematics from Lviv Polytechnic National University, Ukraine in 1989, a PhD in 2006. Since 2009 he has been an Associate Professor of the Department of Computerized Automatic Systems at Lviv Polytechnic National University, Ukraine. Her research interests include evolutionary models, numerical methods, and digital signal processing. ORCID: 0000-0003-0529-8582.

Andrii Pavelchak received an M.S. in Automation from Lviv Polytechnic National University, Ukraine in 1999, a Ph.D. in 2007. Since 2011 he has been an Associate Professor of the Department of Computerized Automatic Systems at Lviv Polytechnic National University, Ukraine. His research interests include evolutionary models, and numerical methods. ORCID: 0000-0003-3898-1556.